

TOP SECRET

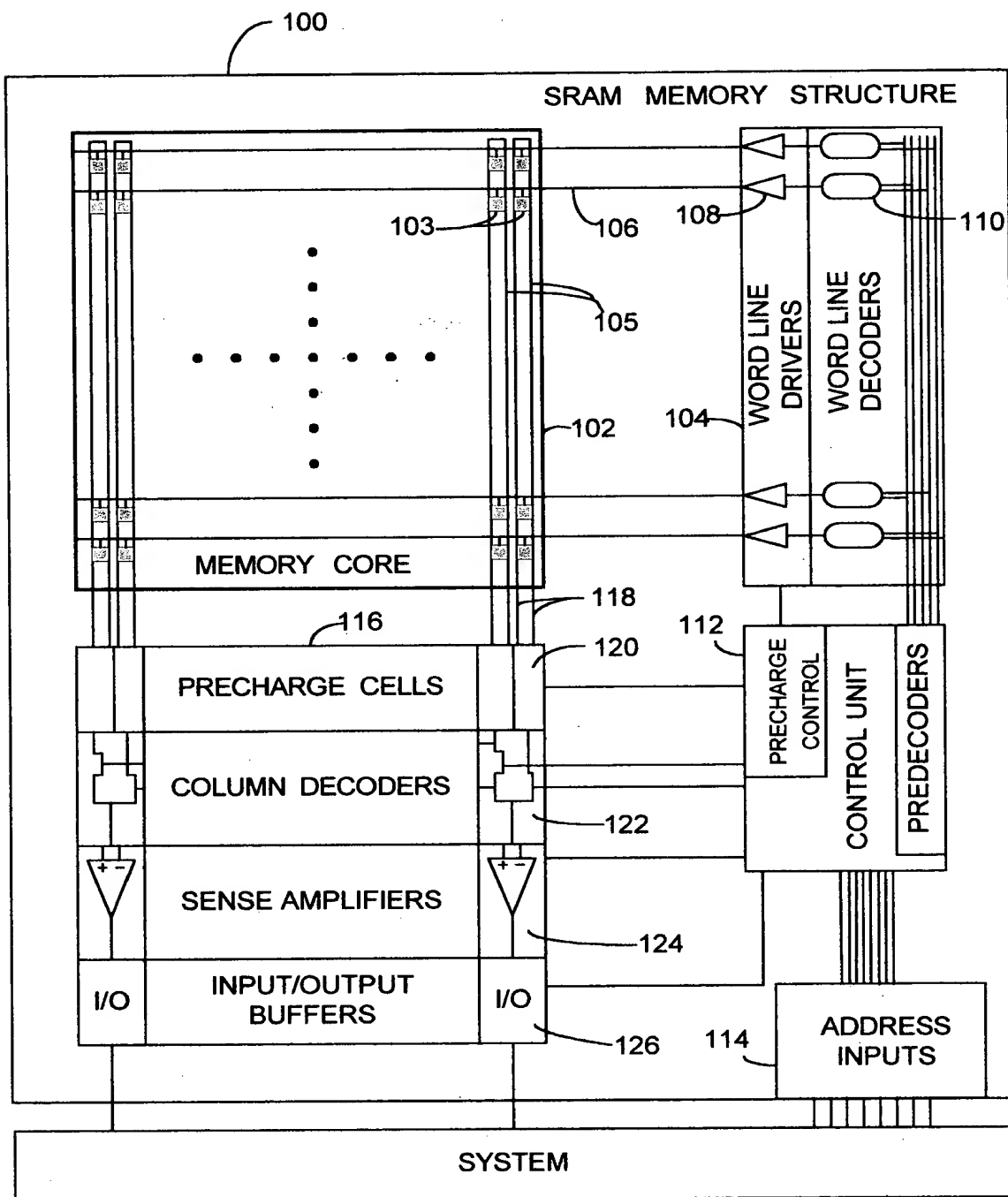


FIG. 1

The diagram illustrates a Six-Transistor CMOS SRAM Cell (200). The cell is connected to a V_{DD} supply and a ground symbol. It features four access transistors (201a, 201b, 201c, 201d) and two storage capacitors (206, 208). The word line (204) is connected to the gates of the access transistors. The bit line (202) is connected to the storage capacitors. The diagram is labeled "SIX-TRANSISTOR CMOS SRAM CELL".

FIG. 2

FIG. 3

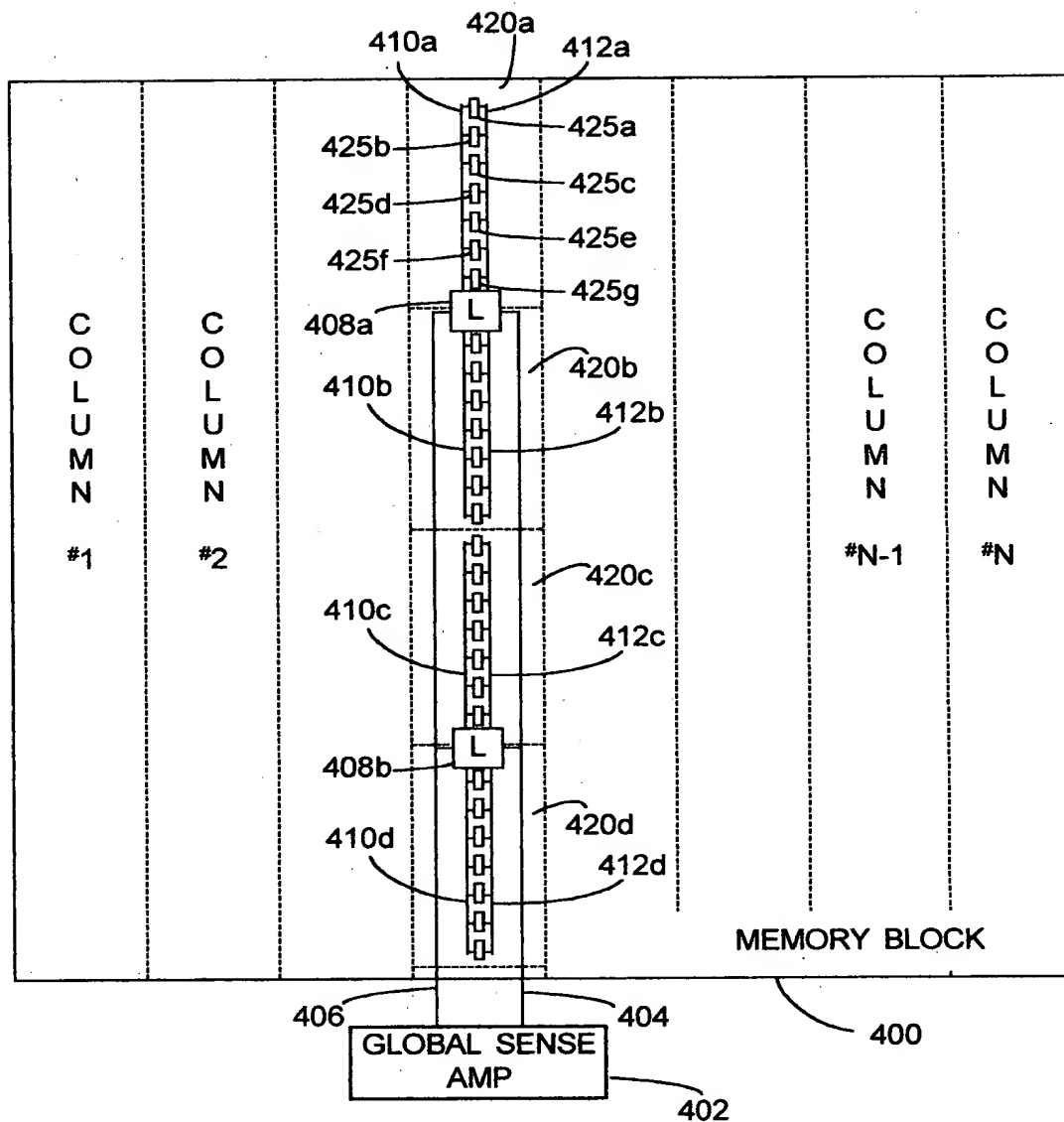


FIG. 4

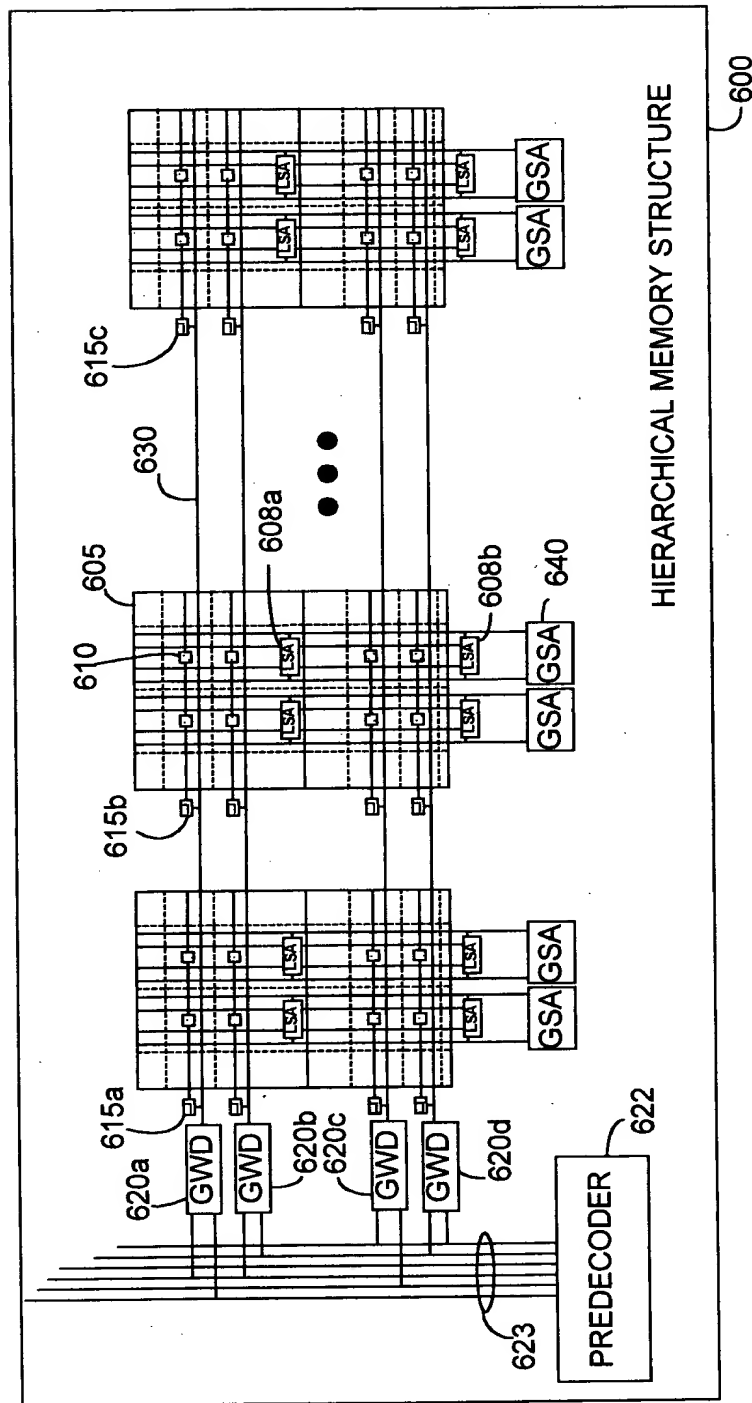


FIG. 6

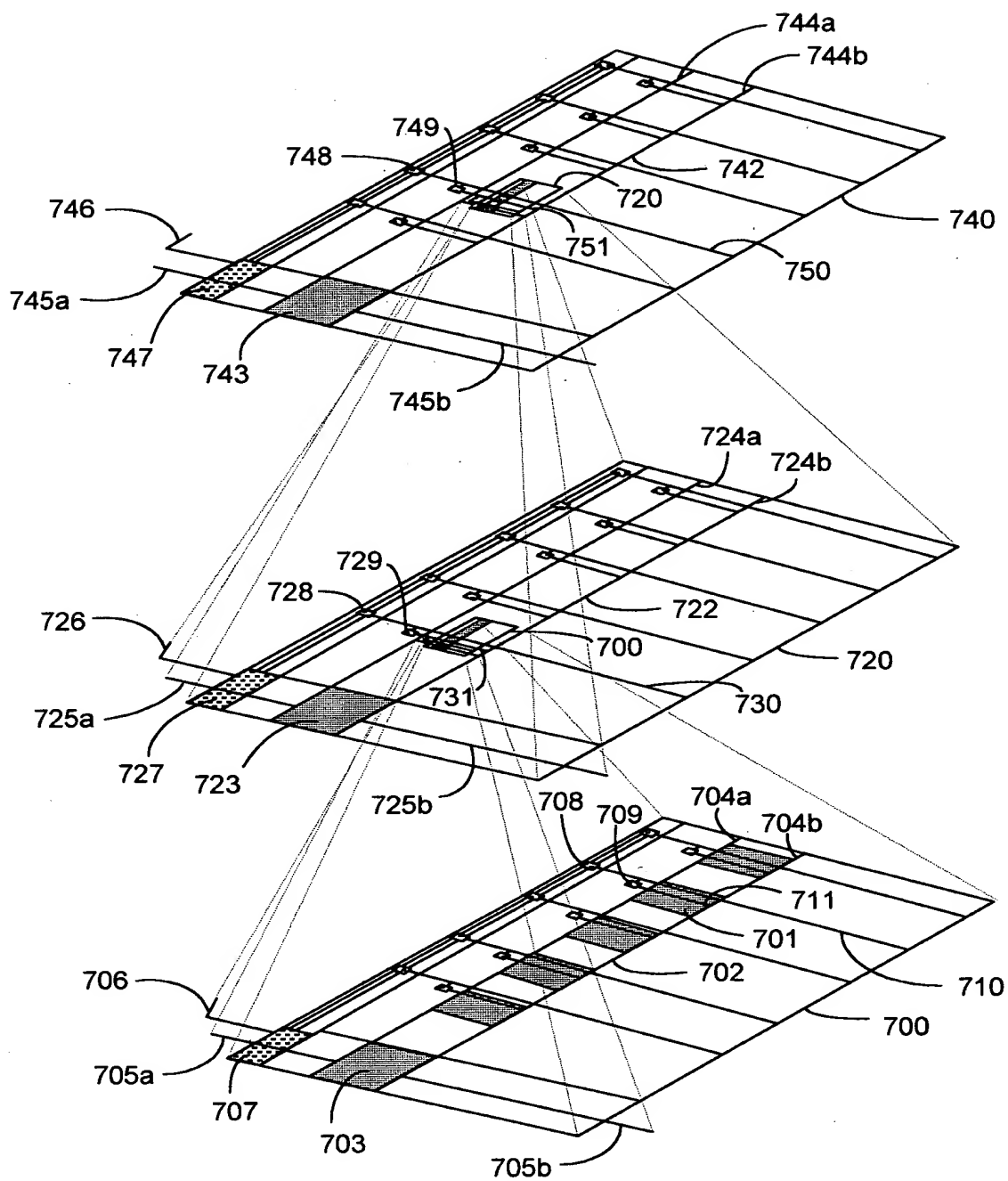


FIG. 7

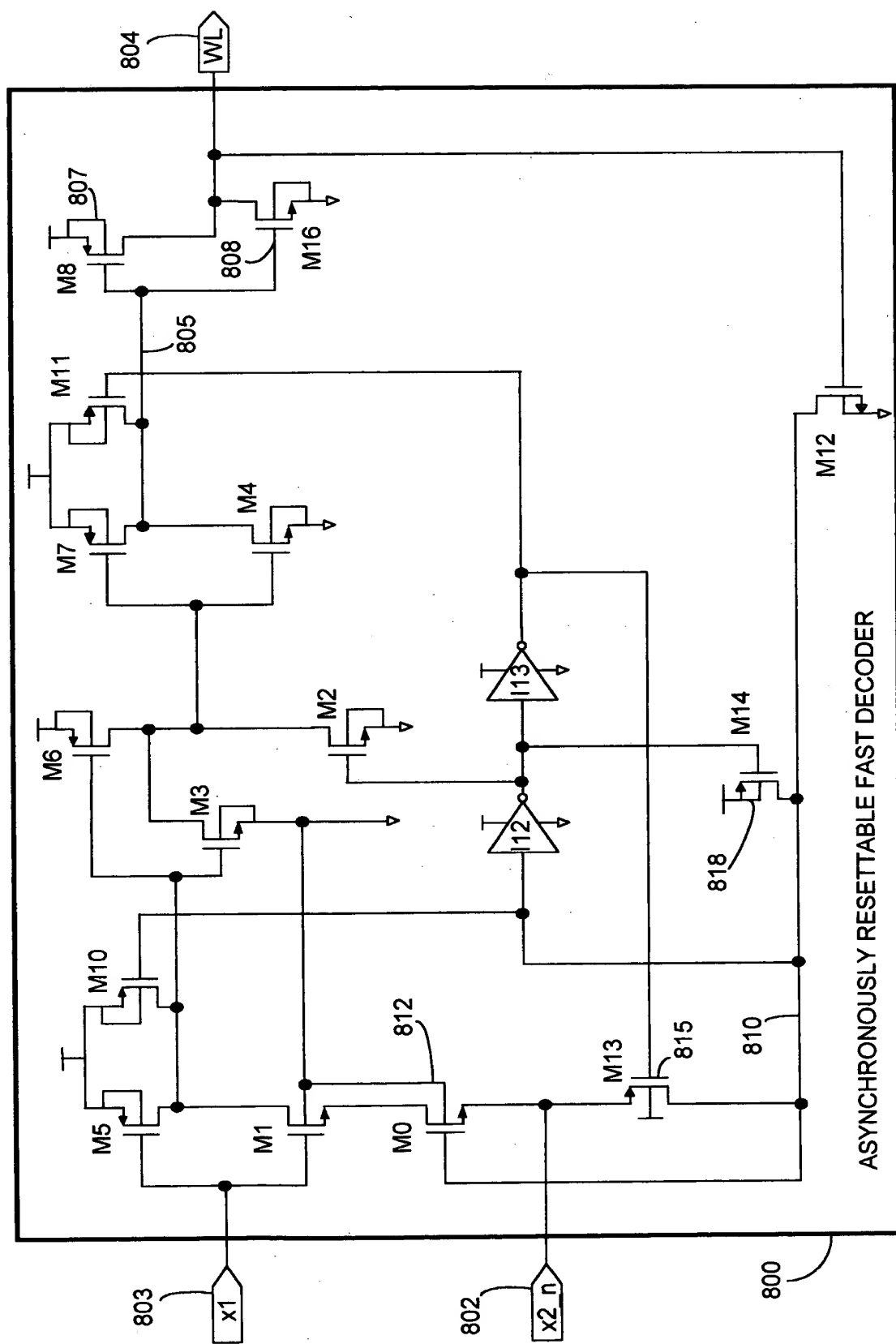


FIG. 8

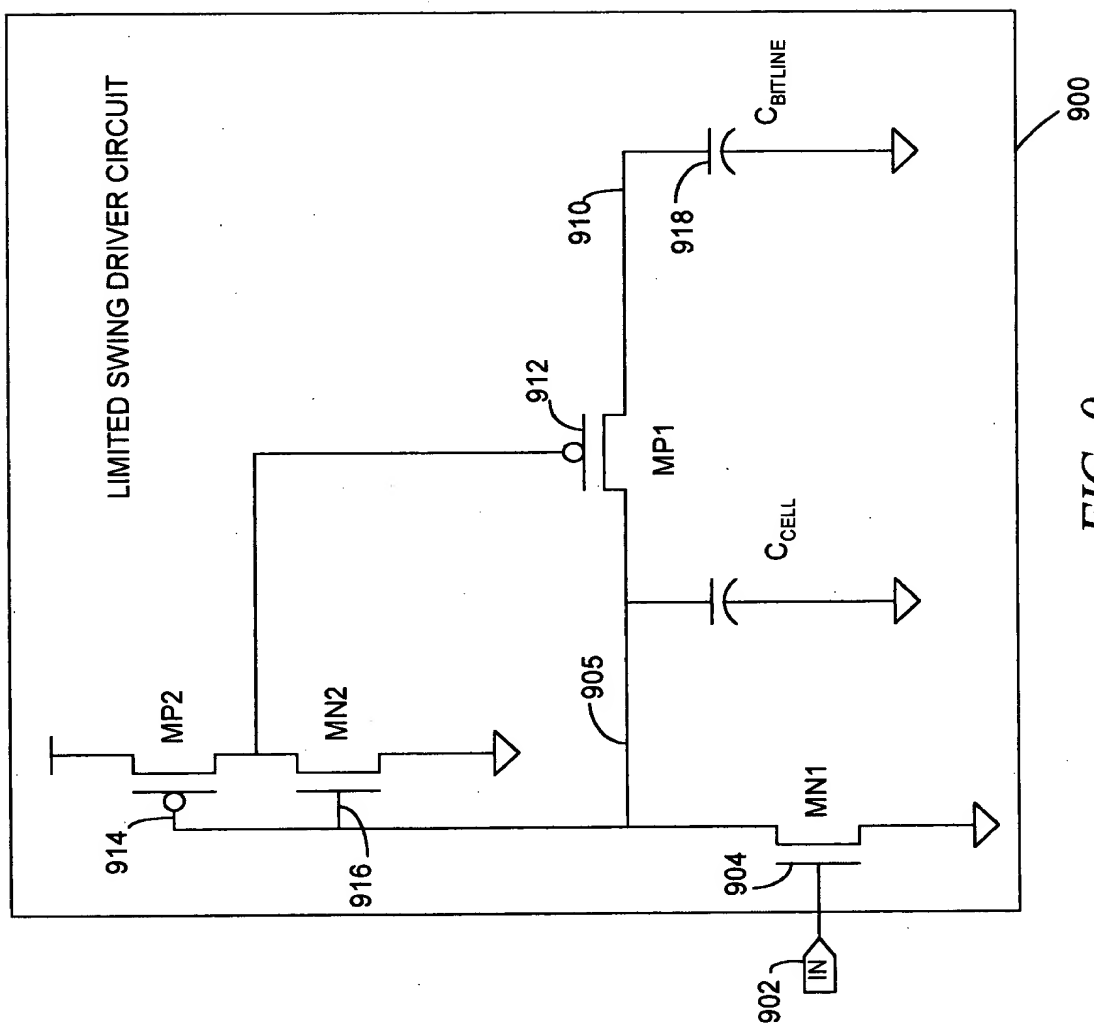


FIG. 9

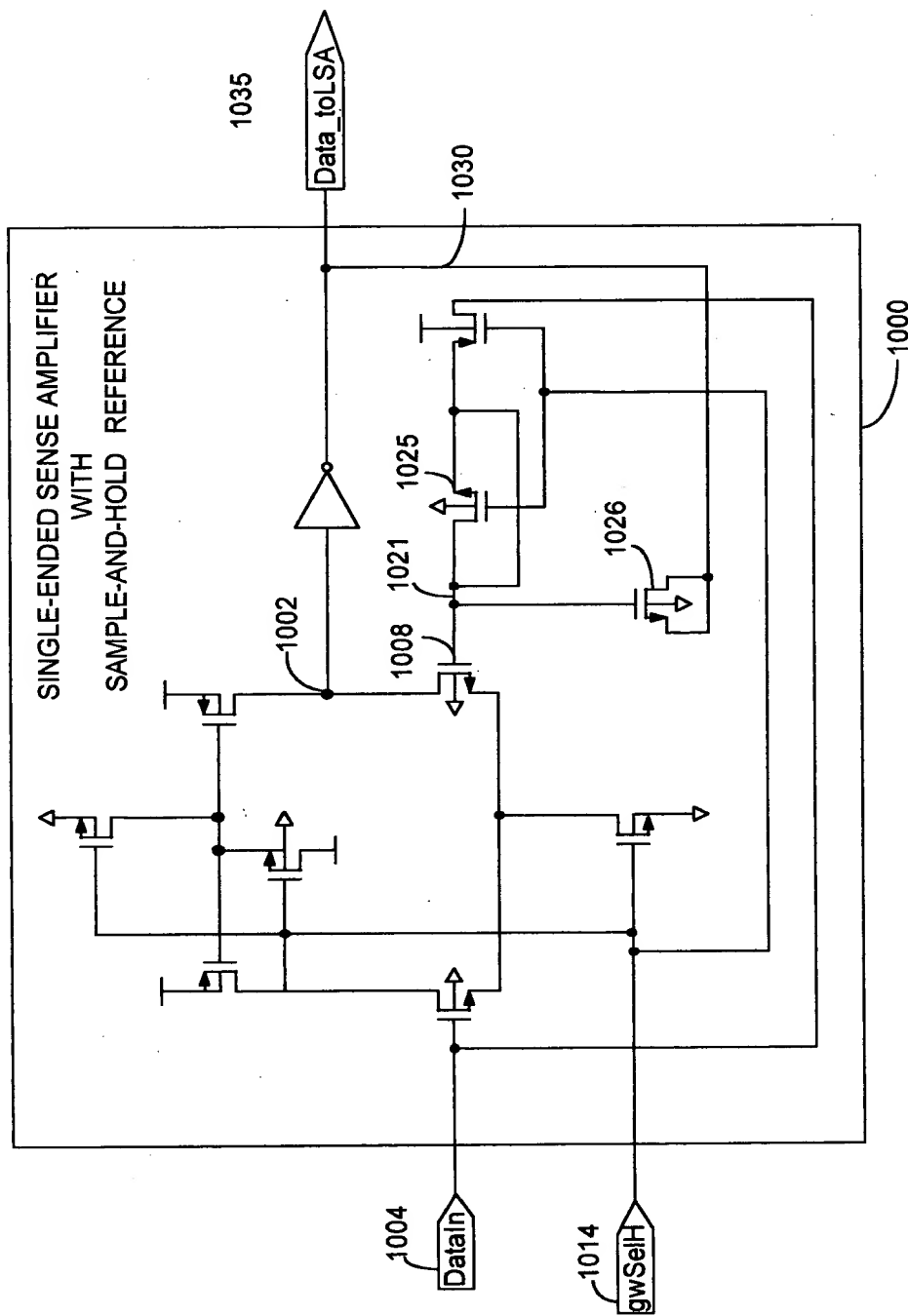


FIG. 10

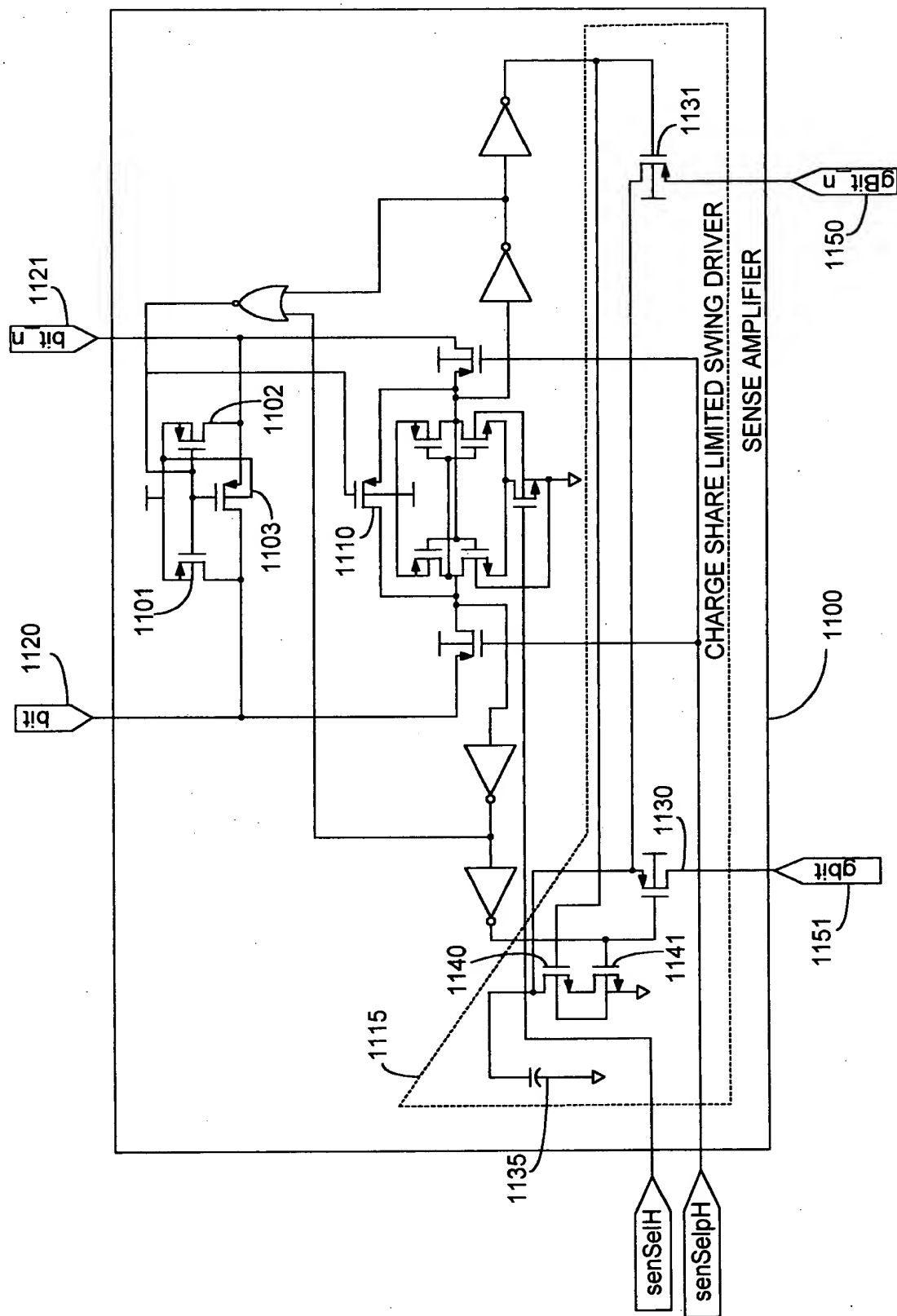


FIG. 11

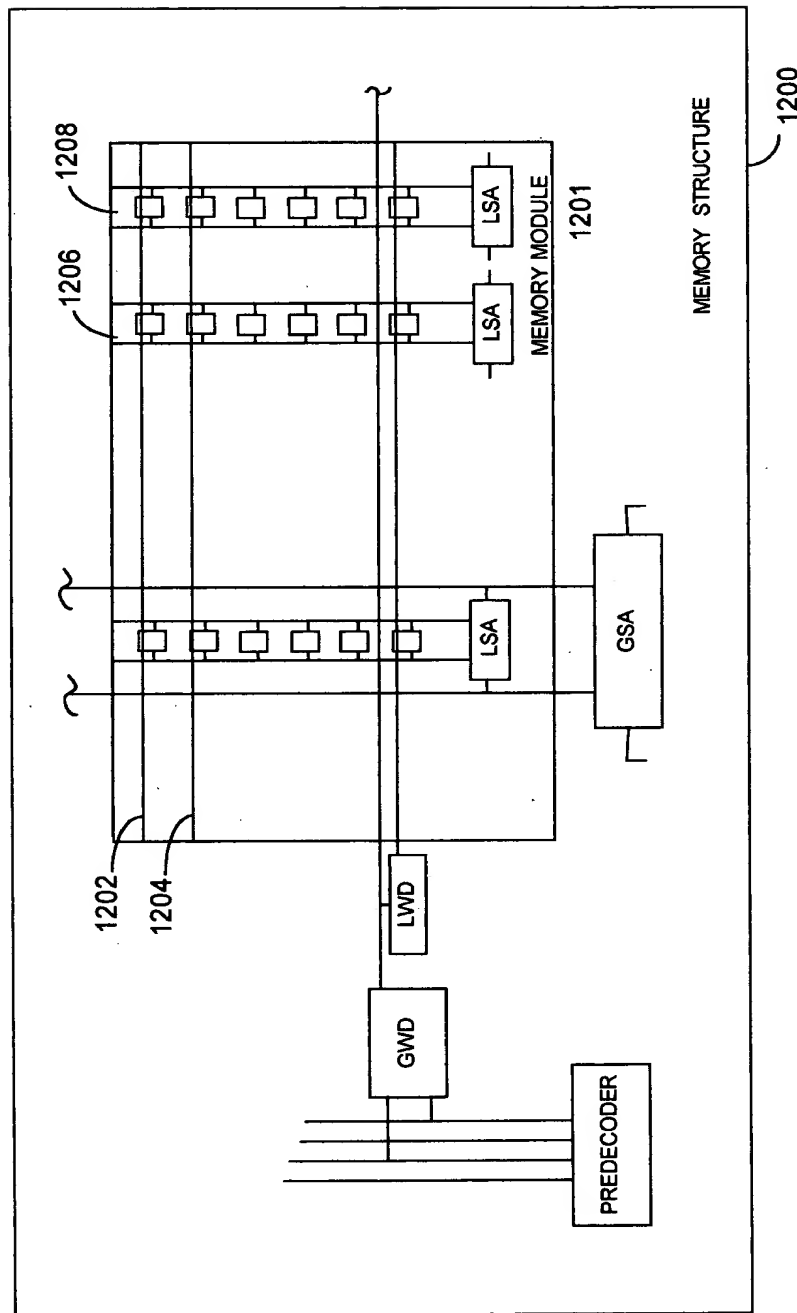


FIG. 12

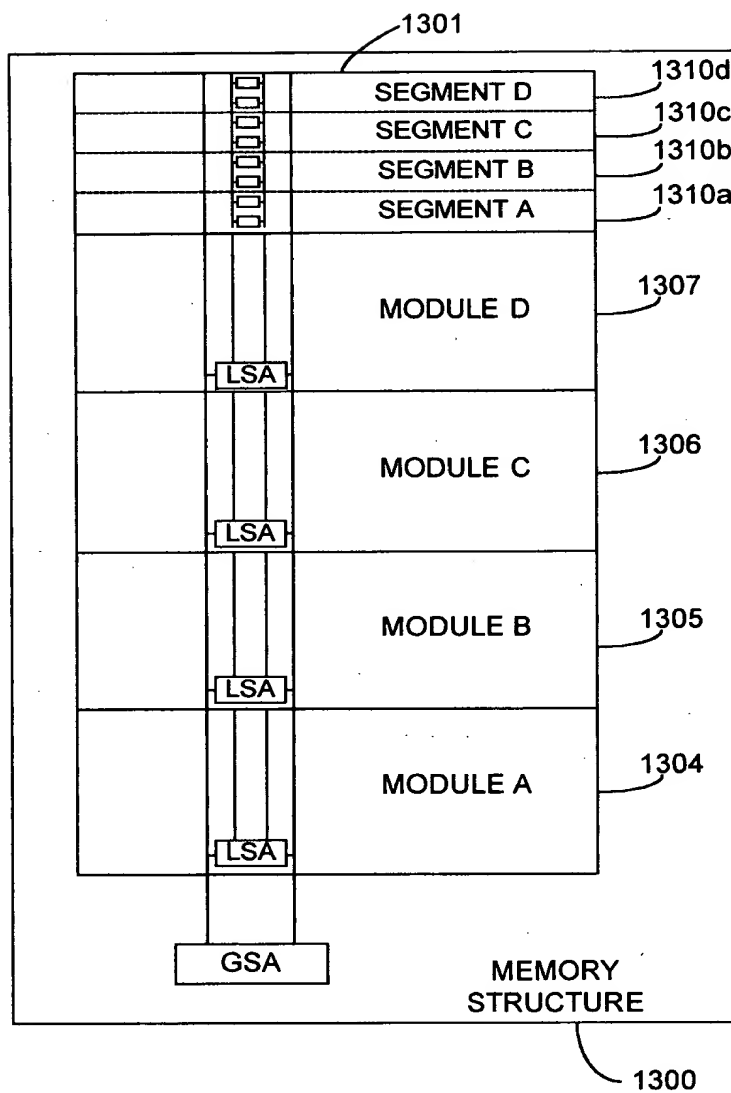


FIG. 13

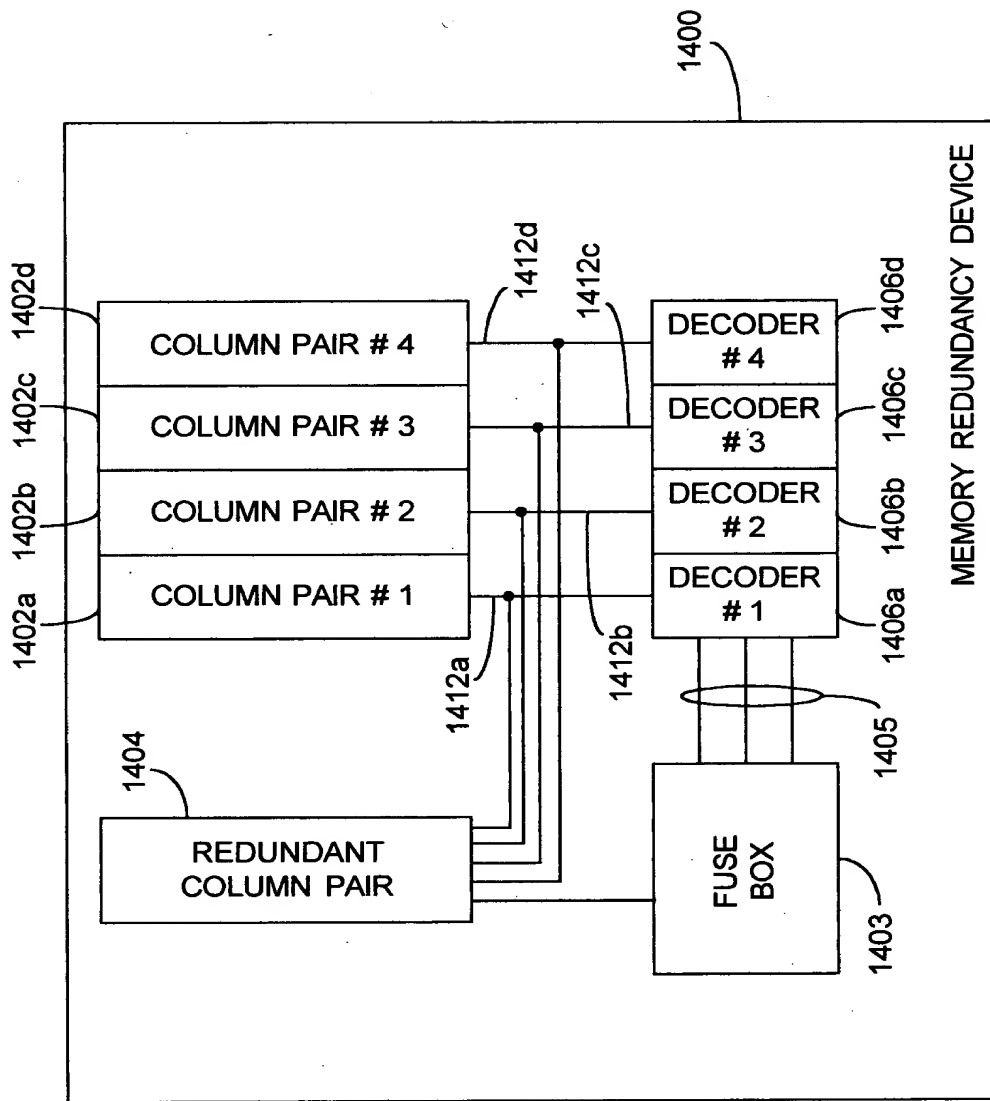


FIG. 14

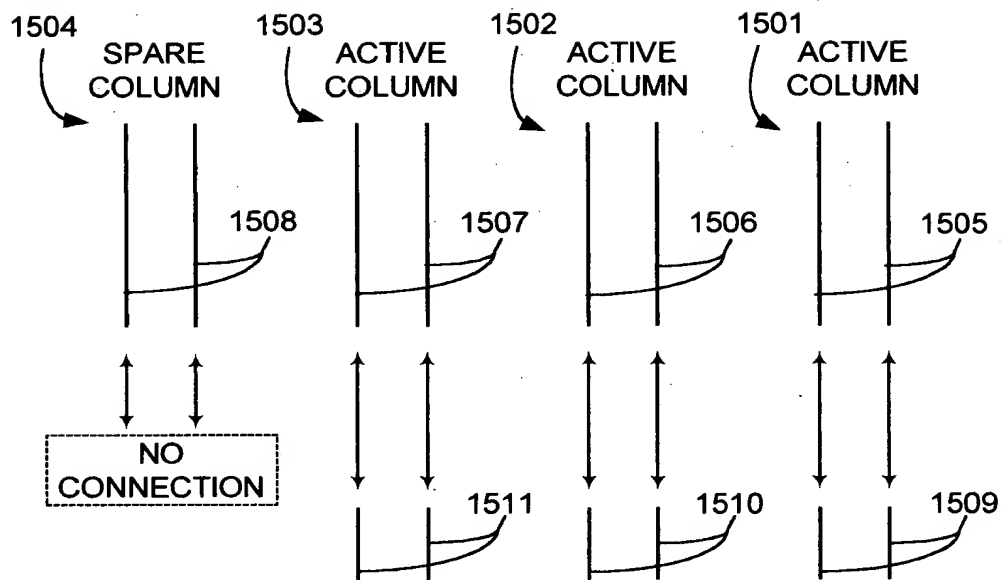


FIG. 15A

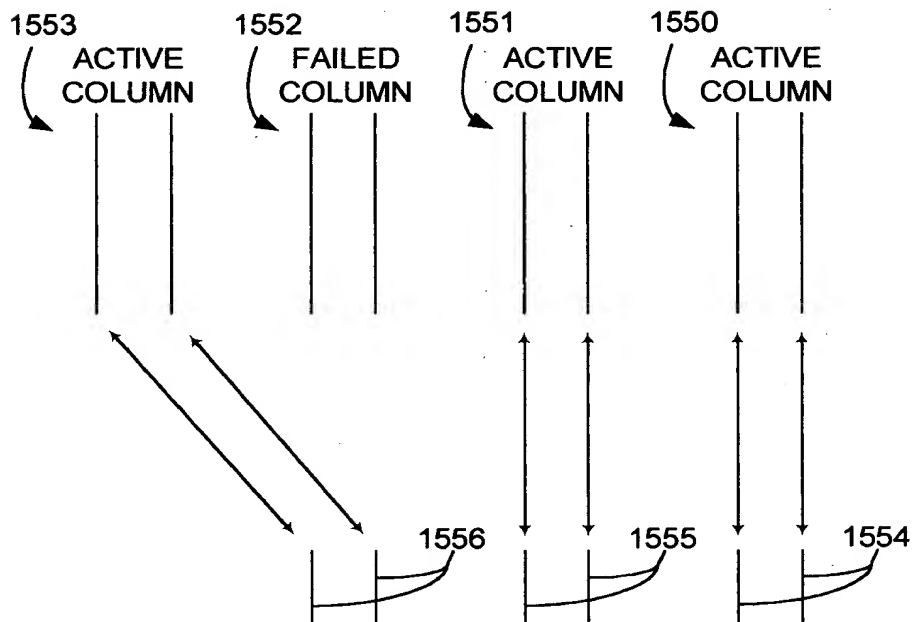


FIG. 15B

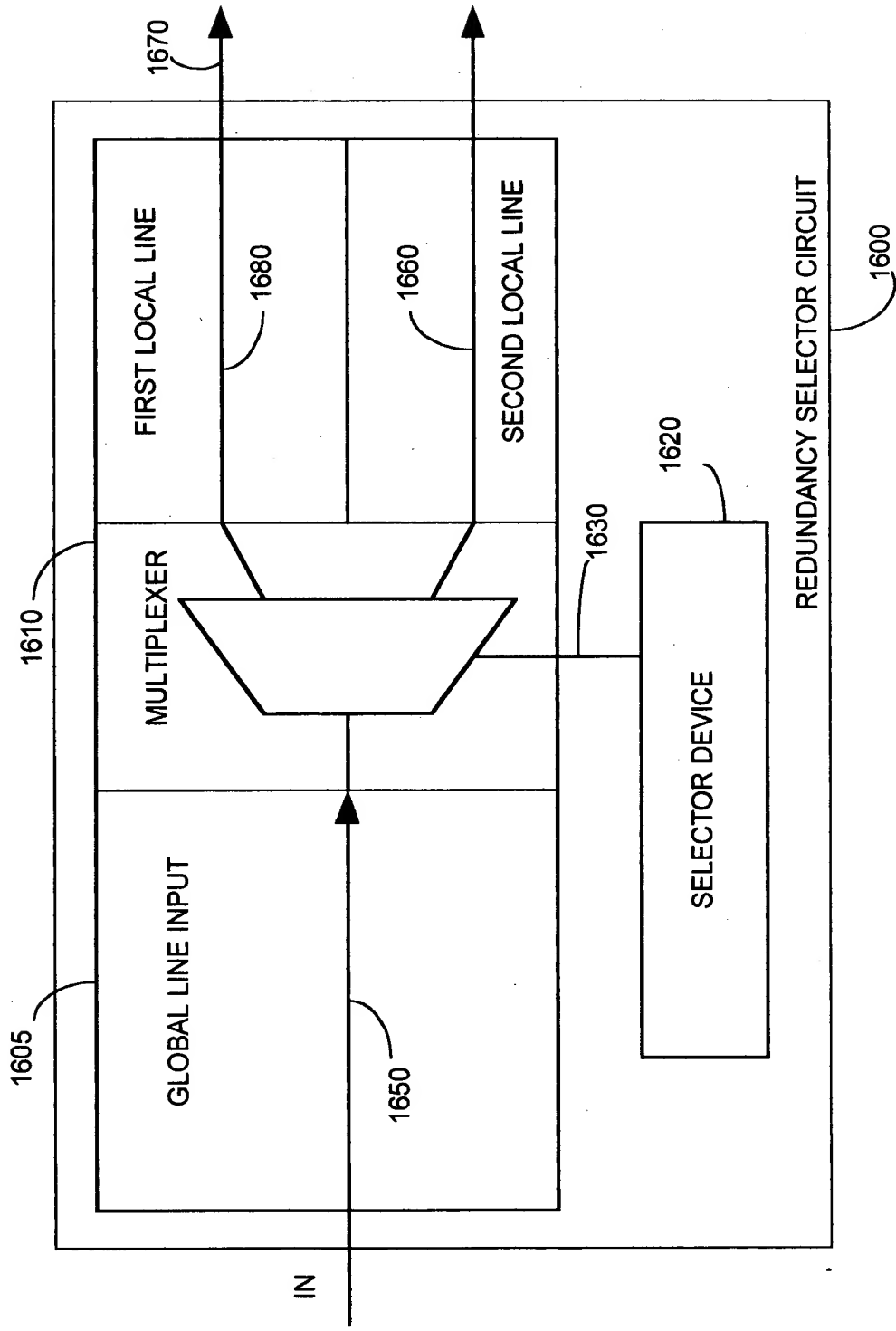


FIG. 16

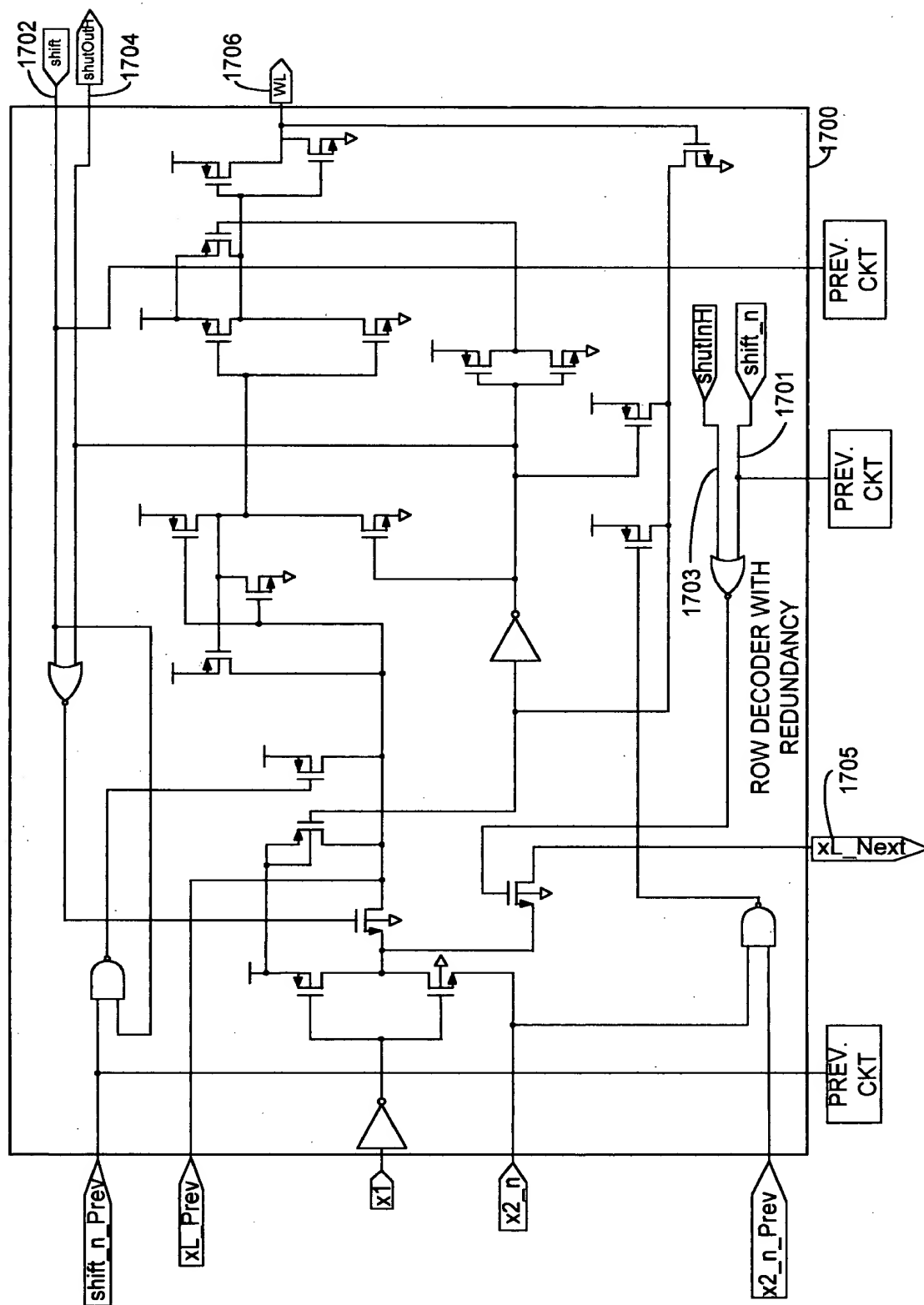


FIG. 17

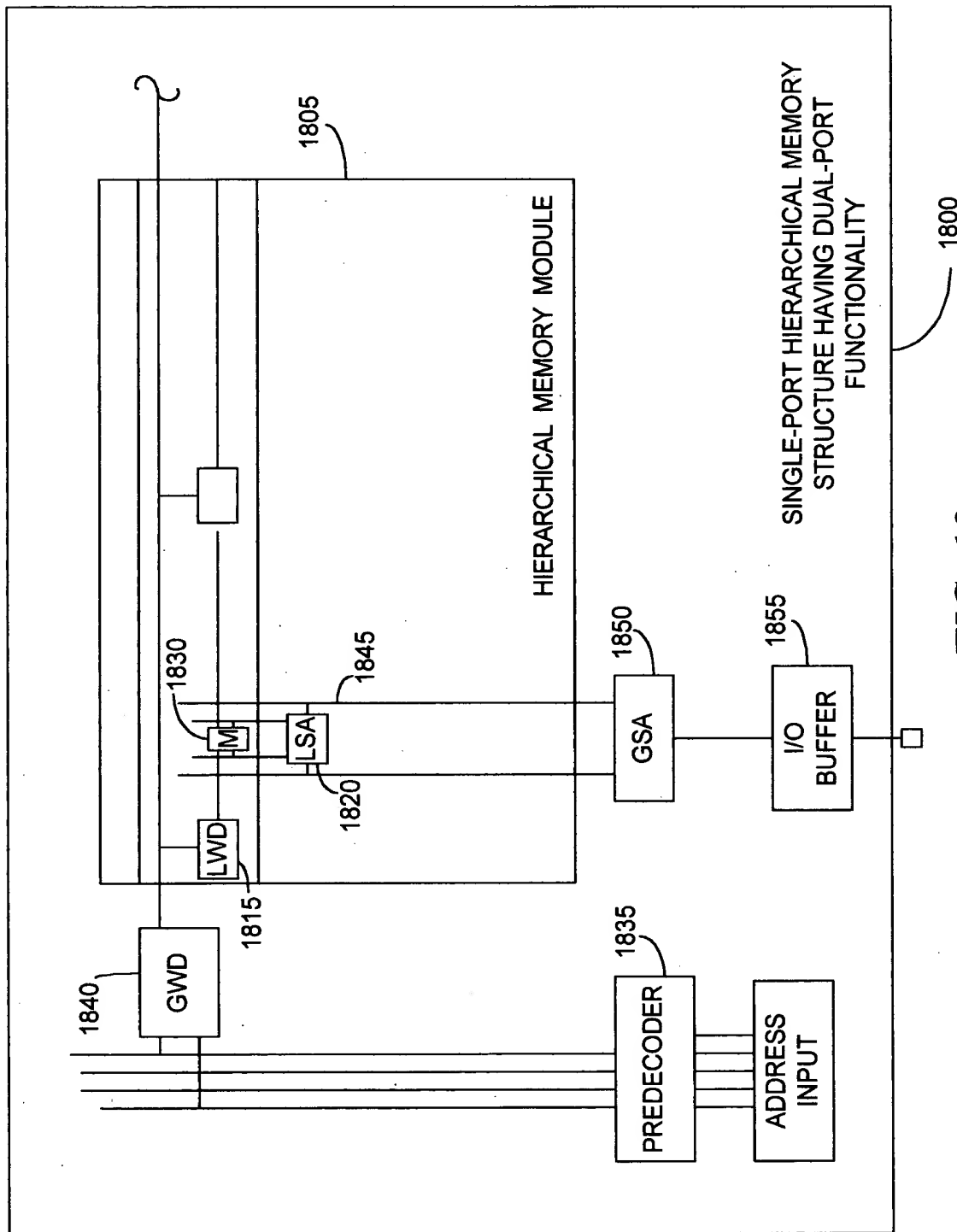


FIG. 18

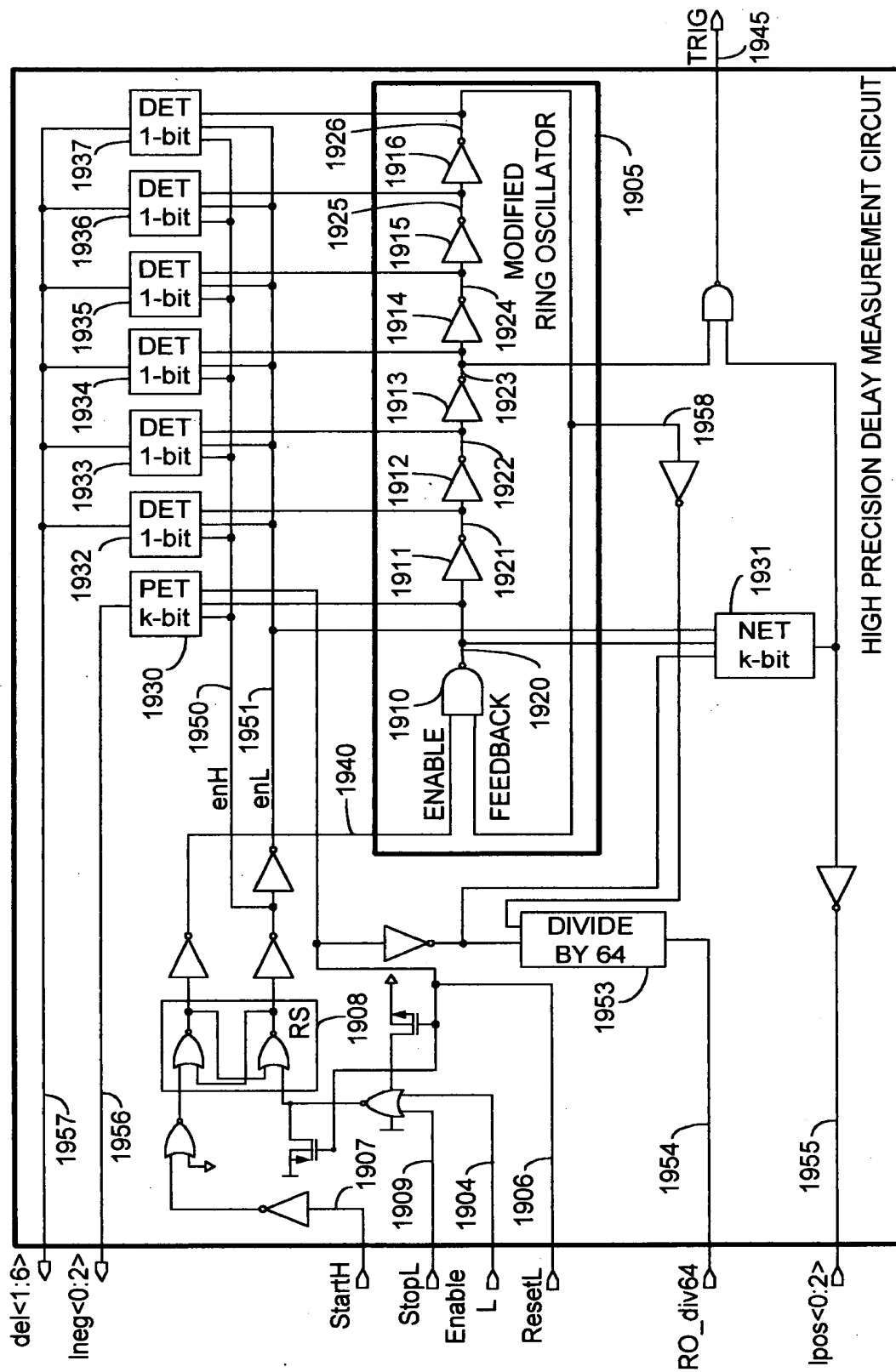


FIG. 19

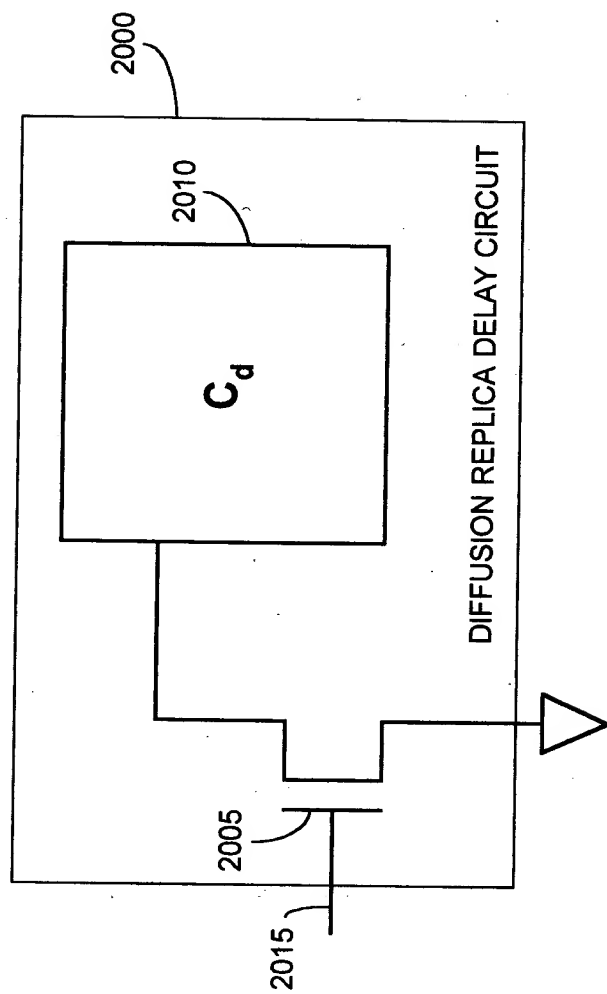


FIG. 20

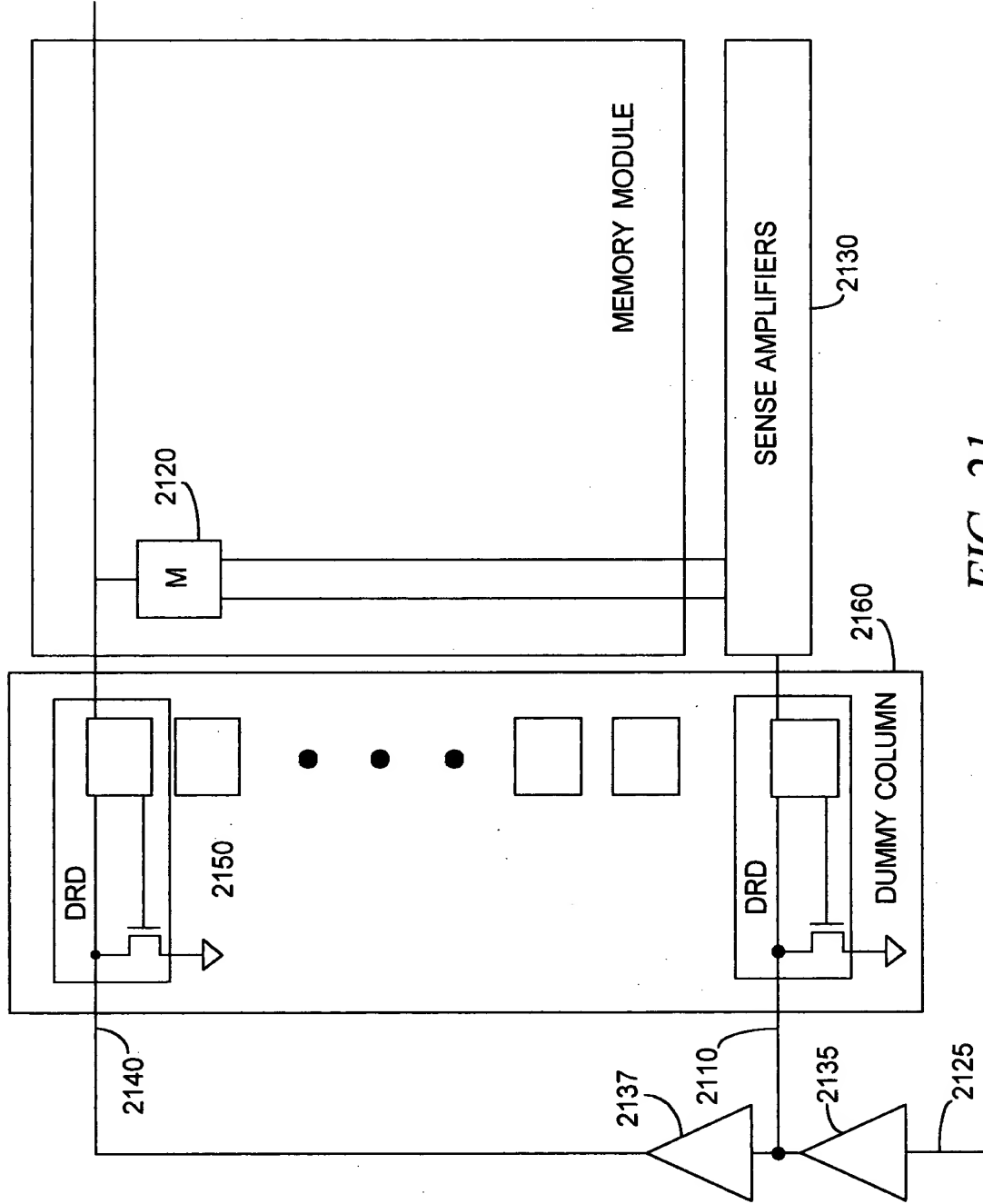


FIG. 21

FIG. 22A

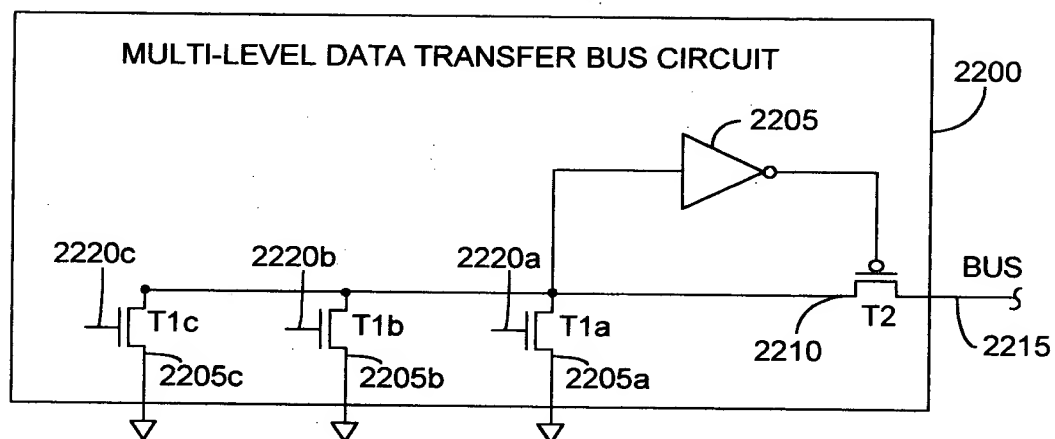


FIG. 22A

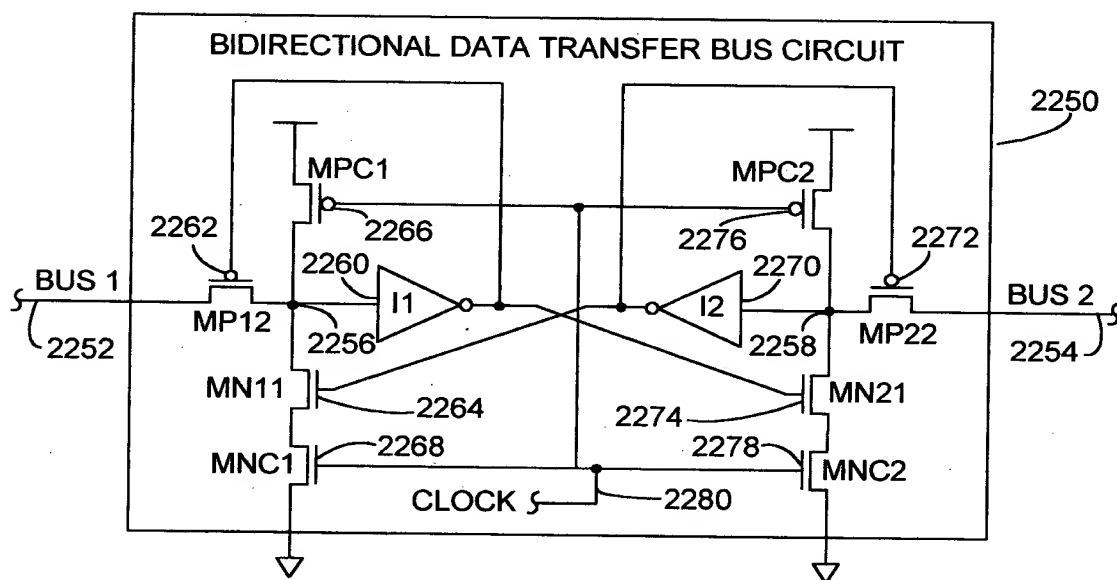


FIG. 22B